**Description**

TRC2441-1CGA is a single 2.5/1.25 Giga bit per second Passive Optical Network (GPON) OLT serializer/deserializer (SerDes) IP core with Burst Mode Clock Data Recovery (BMCDR) over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device supports a downstream data rate of 2.488 Gbps and 1.244 Gbps, upstream data rate of 1.244 Gbps, and is ITU GPON (G.984.2) compliant interface. TRC2441-1CGA operates from 1.0/2.5 V supplies and has power management with several power down modes.

The transmit section of TRC2441-1CGA contains a low-jitter clock synthesizer derived from the CDR block, a parallel to serial converter and a CML output driver with selectable pre-emphasis for use in Optical Line Termination (OLT) SoC central office or other GPON applications. The receive section contains an input limiting amplifier with on-chip auto calibration terminations and four (4) selectable equalization levels, Burst Mode Clock Data Recovery (BMCDR) PLL using a reference clock, built-in serial loop-back modes, PRBS generator/checker and error detector aid in support of testing and debugging.

TRC2441-1CGA's high jitter tolerance is ideal for use in SoCs and ASICs in the presence of multiple clocks and noise.

**Features**

- Downstream speed: 2.488 Gbps/1.244 Gbps
- Upstream speed: 1.244 Gbps
- ITU GPON OLT compliant (G.984.2)
- Fast Burst Mode Clock Data Recovery (BMCDR) - less than 12 bits
- High-speed differential reference clock
- Jitter Tolerance and Jitter Generation exceed standard
- High-speed serial CML output drivers with internal selectable 50 Ω terminations
- Input stage with internal 50 Ω terminations
- Termination resistor auto calibration
- Option for crystal osc. or clock driver
- Supports De-emphasis on the serial output drivers (optional)
- Supports up to four levels of equalization at the serial inputs
- Loss of signal indicator (LOS)
- Local and Remote loopbacks
- Pseudo-Random (2^7 PRBS) pattern generator and error checker to support BIST
- Supply Voltage: 1.0 V/2.5 V ±5%
- Power dissipation: less than 100 mW
- Chartered advanced 90 nm G CMOS process
- Portable to other processes

**Application**

Passive Optical Networks – GPON/EPON
WDM Transponders
Test Equipment

**Figure 1: System Application**
**General Description**

TRC2441-1CGA consists of transmit and receive paths. Serial data arrives at the input receiver amplifier, after amplification it passes through an equalizer and a slicer. The analog input data is monitored in amplitude to indicate the loss of signal (LOS). The output of the slicer is used by the burst mode clock data recovery (BMCDR) to extract the clock and realign the data. To support BMCDR, TRC2441 has a very fast PLL lock time (less than 12 bit).

A frequency locked loop is used to lock to the incoming data fast to determine the received data carrier frequency then a phase locked loop acquire phase lock and track the received data. A lock indicator circuit is used to indicate that CDR PLL is tracking the incoming data. The serial data is converted to parallel data by the deserializer block.

The 8-bit or 16-bit parallel data is probed by a pattern checker, which is used in test mode to evaluate the channel and error rate.

On the transmit path, parallel data stream are converted to serial data. The serial data signal is clocked and transmitted to the transmit data alignment block and are sent to the driver block and transmitted on the media through high-speed output block.

The reference clock is used by the transmitter phase locked loop (TX-PLL) to generate the TX data and align the TX data before the driver. The divider-select signal can be programmed by the serial interface to select the TX clock data rate.

TRC2441-1CGA has a built-in-self-Test (BIST) to generate many different pseudo random bit stream (PRBS) patterns to test the transmitter and receiver blocks. TRC2441-1CGA has Near-End and Far-End loop-backs for testing and debugging. The loop-backs allow local and remote system level testing.