

Quad 1.06/2.125 Gbps Fibre Channel SerDes IP Core

Description

TRC2104CFA is a Quad serializer/deserializer (SERDES) transceiver device IP core, delivering high-speed serial data transmission over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device offers four independent channels delivering high speed bi-directional point-to-point baseband data transmission, which can be utilized for a variety of applications. TRC2104CFA operates on a single 1.8v supply. The device is capable of transmitting and receiving serial data at 1.0625/2.125Gbps, per channel.

Each transmit section of the TRC2104CFA contains a low-jitter clock synthesizer, a parallel to serial converter with built-in 8b/10b encoder, and a CML output driver with selectable pre-emphasis for use in backplane applications.

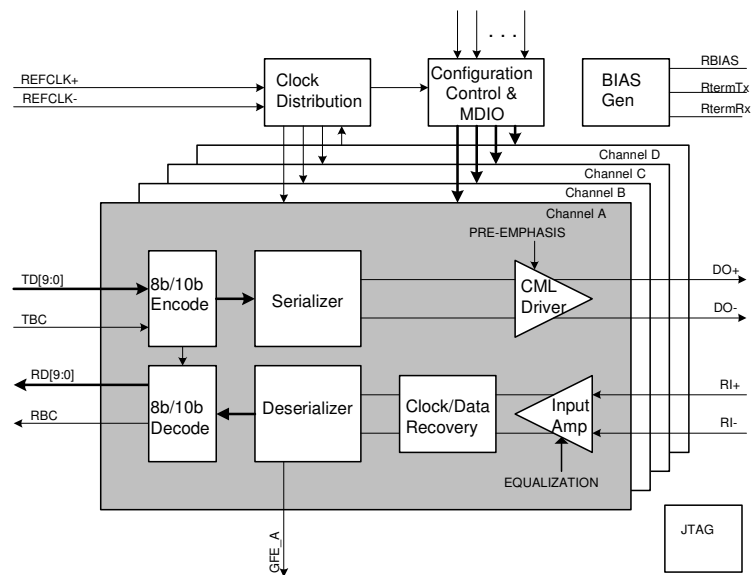
Each receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, clock/data recovery PLL, Comma detector, and a serial to parallel converter with built-in 8b/10b decoder. A built-in serial loopback mode, PRBS generator/checker and error detectors aid in support of testing.

The TRC2104CFA requires no external components for its clock synthesizers and clock recovery PLL's. Three external resistors are needed to set the proper bias currents for its on-chip terminations.

Features

- Quad SERDES optimized for Fibre Channel/Gigabit Ethernet applications
- Data rates from 1.0625 to 3.125Gb/s
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- Jitter performance exceeds Fibre Channel spec.
- On-chip 8b/10b encoders and decoders
- High speed serial CML output drivers with internal 50 Ω terminations
- High speed serial CML input stage with internal 50 Ω terminations
- Auto-calibration termination
- Supports up to four levels of pre-emphasis on the serial output drivers
- Supports up to four levels of equalization at the serial inputs
- Comma Detect for character alignment
- Local serial loopback test mode
- Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial interface MDIO
- Single 1.8V \pm 5% supply for parallel and high speed serial I/O interfaces
- Power dissipation: 400 mW/Ch
- TSMC advanced 0.18um CMOS process

Figure 1. General Function Diagram



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Figure 2. Functional block diagram

