GPON ONU SerDes IP Core

Description

TRC2441 is a single Gig-bps Passive Optical Network (GPON) serializer/deserializer (SerDes) IP core, delivering high-speed serial data transmission over controlled impedance transmission media such as copper cable, PCB traces or fiber optics. The device offers a downstream data rate of 2.488 Gbps, 1.244 Gbps, and upstream data rate of 1.244 Gbps, is ITU GPON (G.984.2) compliant interface. TRC2441 operates from 1.0/2.5 V supplies. The device is capable of transmitting and receiving asymmetrical serial data up to 2.5 Gbps.

The transmit section of TRC2441 contains a low-jitter clock synthesizer derived from the receive clock data recovery block, a parallel to serial converter, and a CML output driver with selectable de-emphasis for use in Optical Network Unit (ONU) and Optical Line SoC and equipment and other GPON applications.
The receive section contains an input limiting amplifier with on-chip terminations and selectable equalization level, clock/data recovery PLL using a reference clock. Built-in serial loopback modes, PRBS generator/checker and error detector aid in support of testing and debugging.
TRC2441's high jitter tolerance is ideal for use in SoCs and ASICs in the presence of multiple clocks and noise.

Application

Passive Optical Networks – GPON
WDM Transponders
Test Equipment

Features

- Downstream speed: 2.488Gbps/1.244Gbps data rate
- Upstream speed: 1.244Gbps
- ITU GPON ONU compliant (G.984.2)
- 19.44 MHz reference clock
- Jitter Tolerance and Jitter Generation exceed standard
- High-speed serial CML output drivers with internal 50 Ω terminations
- input stage with internal 50 Ω terminations
- Supports De-emphasis on the serial output drivers (optional)
- Supports equalization at the serial inputs
- 8b laser driver control signal path with less than 1b delta latency with data path
- Local and Remote loopbacks
- Pseudo-Random (2^7 PRBS) pattern generator and error checker to support BIST
- Supply Voltage: 1.0 V/2.5 V ±5%
- Power dissipation: less than 150 mW
- Chartered advanced 90 nm G CMOS process
- Portable to other processes

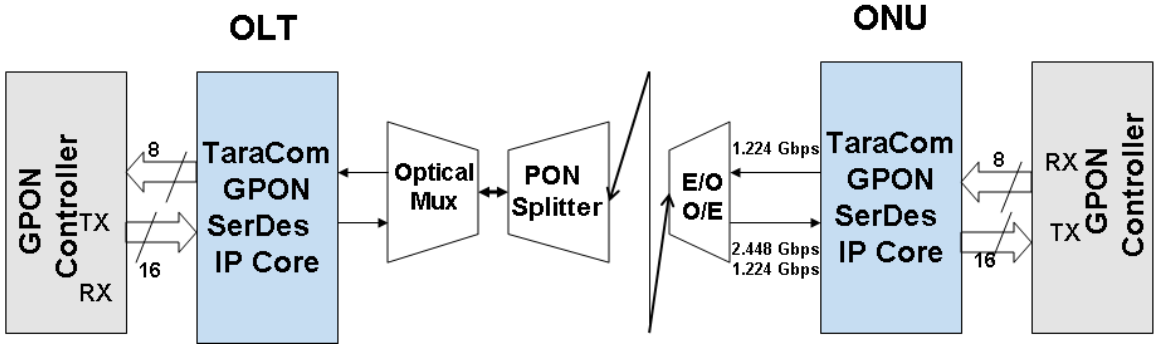
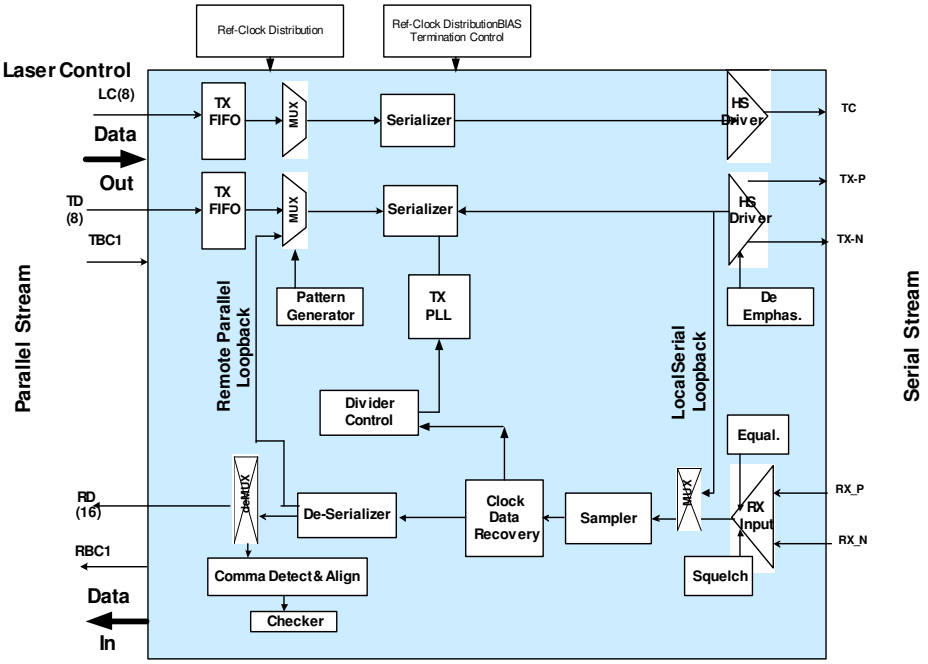


Figure 2. Functional block diagram



General Description

TRC2441 consists of transmit and receive paths. Serial data arrives at the input receiver amplifier, after amplification it passes through an equalizer and a slicer. The analog input data is monitored in amplitude to indicate the loss of signal (LOS). The output of the slicer is used by the clock data recovery (CDR) to extract the clock and realign the data

A frequency locked loop is used to lock to the incoming data to determine the received data carrier frequency then a phase locked loop acquire phase lock and track the received data. A lock indicator circuit is used to indicate that CDR PLL is tracking the incoming data. The serial data is converted to parallel data by the deserializer block.

The 16-bit parallel data is sent to the controller block. The parallel data is also probed by a pattern checker, which is used in test mode to evaluate the channel and error. The recovered Rx clock is used by the transmitter phase locked loop (TX-PLL) to generate the clock needed to serialize the TX data and align the TX data before the driver.

On the transmit path, parallel scrambled data is fed to the serializer block. The serial data signal is clocked and transmitted to the transmit data alignment block and are sent to the driver block and transmitted on the media through high-speed output block.

TRC2441 has a built-in-self-Test (BIST) to generate many different pseudo random bit stream (PRBS) patterns to test the transmitter and receiver blocks. TRC2441 has local and remote loop-backs for testing and debugging. The loop back blocks allow local and remote system level testing.