Dual Parallel to Serial ATA 1.5/3.0Gb/s Phy IP Core

Description

TRC3002CSA is a Dual Serial ATA (SATA) Host PHY core for interfacing serial data between Storage Device and external 2-port PHY. TRC3002CSA uses double data rate (DDR) transmission for send and receive side. Same Device can operate as a Serial ATA Gen I at 1.5Gb/s and at 3Gb/s Serial ATA Gen 2. Spread Spectrum Clock (SSC) is used to minimize EMI and increase the quality of received signal. It can transmit and receive through a 40-inch cable.

Each transmit section of the TRC3002CSA contains a low-jitter clock synthesizer, an 8-bit or 10-bit parallel to serial converter with built in 8b/10b encoder, and differential high speed Interface output. Its receive section contains an input limiting amplifier with on-chip terminations, a clock/data recovery PLL, a Comma detector, a serial to parallel converter with built-in 8b/10b decoder. OOB circuitry complies with SATA Gen 1 and Gen 2 Standards, featuring COMRESET/COMINIT, and COMWAKE commands and detection.

TRC3002CSA has a built-in Near and Far End Loopbacks. SLUMBER and PARTIAL Power Down feature minimize the power consumption of device.

TRC3002CSA is fabricated with TSMC's advanced 0.13um LV CMOS logic process, and is portable to other processes.

Features

- Serial ATA fully compliant to Gen 1 and Gen 2 SATA Phy Standard.
- Single and Dual data rate capable of transmit and receive at 1.5Gbps and 3.0 Gbps.
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- Jitter Tolerance is better than Specifications.
- 8bit/ or 10bit parallel Core logic.
- 8b/10b encoder and decoder
- High speed serial drivers
- High speed serial input stage with on-chip terminations
- Comma Detect for character alignment
- Far and Near End serial loopback test modes.
- Multi pattern generator and PRBS error checker to support BIST
- Three programmable levels of pre-emphasis and equalization.
- Standard OOB sequencing with optional bypassing OOB capability.
- 1.0V ±5% Supply for logic core and control I/O.
- 1.5V HSTL / or 1.0 V Parallel I/O (optional).
- Low power, 100 mW max per channel.

Application Example:
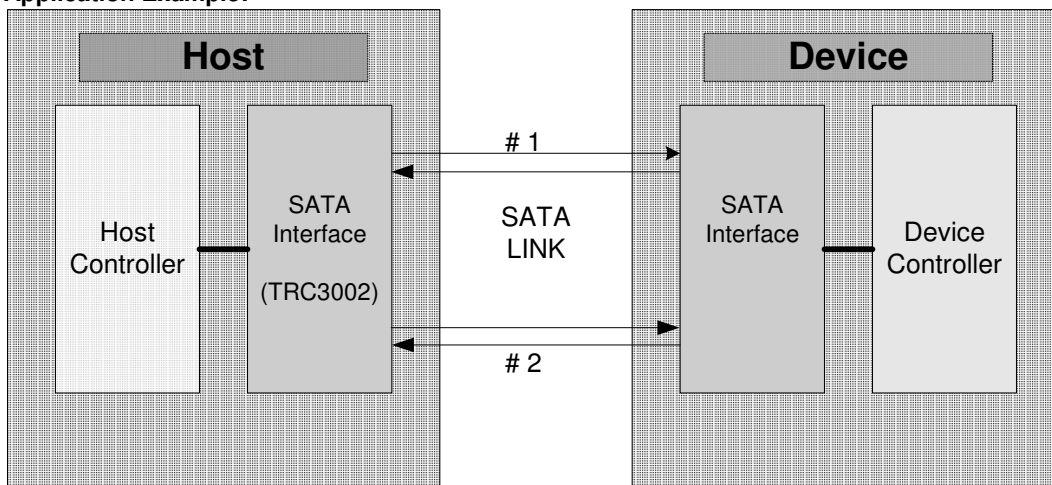
Host: Storage System, Mother Board   Device: Disk Drive, Storage System

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Functional block diagram