1.06/2.125/4.25 Gbps Fibre Channel and Backplane SerDes IP Core

Description

TRC4204CFA is a Quad serializer/deserializer (SerDes) IP Core for high-speed serial data transmission for Fiber Channel applications as well as backplane requirements over controlled impedance transmission media such as twin-axial cable or printed circuit board. It is capable of transmitting and receiving serial data at 1.0625/2.125/4.25 Gb/s.

Each transmit section of the TRC4204CFA contains a low-jitter clock synthesizer, an 8-bit or 10-bit parallel to serial converter with built in 8b/10b encoder, and differential high speed CML output drivers with selectable pre-emphasis optimized for backplane applications. Its receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, a clock/data recovery PLL, a Comma detector, a serial to parallel converter with built-in 8b/10b decoder.

A built-in serial loopback mode, PRBS generator/checker and error detectors aid in support of testing.

TRC4204CFA requires no external components for its clock synthesizers and clock recovery PLLs. Three external resistors are needed to set the proper bias currents, and to compensate for process variations to achieve tight tolerance on its on-chip terminations. TRC4204CFA is fabricated with TSMC's advanced 90 nm CMOS logic process, Each receive section contains an input limiting amplifier with on-chip terminations and selectable equalization levels, clock/data recovery PLL, Comma detector, and a serial to parallel converter with built-in 8b/10b decoder.

Features

- Quad SerDes optimized for Fibre Channel and backplane applications
- Supports data rates from 1.0625/2.125 and 4.25 Gbps speeds
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- 8b/10b encoder and decoder
- High speed serial CML output drivers with internal 50 Ω terminations
- High speed serial CML input stage with internal 50 Ω terminations
- Auto-calibration termination
- Supports up to four levels of pre-emphasis on the serial output drivers
- Supports up to four levels of equalization at the serial inputs
- Comma Detect for character alignment
- Local serial loopback test mode
- Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial interface MDIO
- 1149.1 compatible JTAG port
- 1.0/1.8V ±5% supplies
- Power dissipation 125 mW/Ch
- TSMC advanced 90 nm CMOS process
- Portable to other processes

Figure 1. General Function Diagram

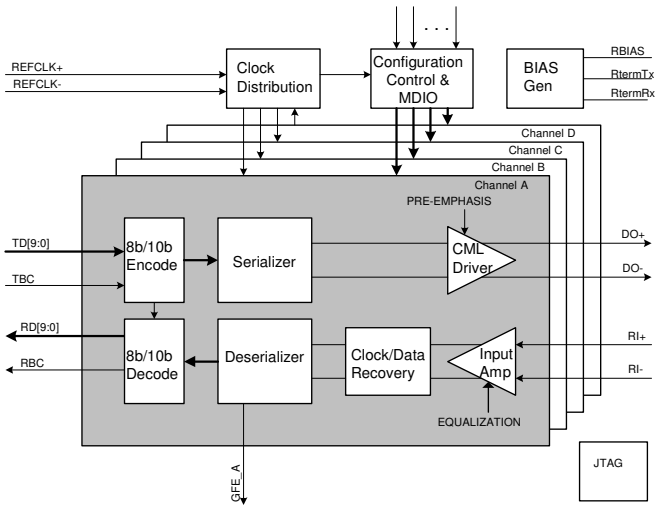

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Figure 2. Functional block diagram