Dual Serial ATA 1.5/3.0/6.0 Gbps Phy IP Core

Description

TRC6002CSA is a Dual Serial ATA (SATA) Host PHY core for interfacing serial data between Storage Device and external 2-port PHY. TRC6002CSA uses double data rate (DDR) transmission for send and receive side. The Device can operate as a Serial ATA Gen I at 1.5 Gbps, Gen 2 at 3.0 Gbps and Gen 3 at 6.0 Gbps. Spread Spectrum Clock (SSC) is used to minimize EMI and increase the quality of received signal. It can transmit and receive through a 40-inch cable.

Each transmit section of the TRC6002CSA contains a low-jitter clock synthesizer, an 8-bit or 10-bit parallel to serial converter with built in 8b/10b encoder, and differential high speed Interface output. Its receive section contains an input limiting amplifier with on-chip terminations, a clock/data recovery PLL, a Comma detector, a serial to parallel converter with built-in 8b/10b decoder. OOB circuitry complies with SATA Gen 1,Gen 2, and Gen 3 Standards, featuring COMRESET/COMINIT, and COMWAKE commands and detection.

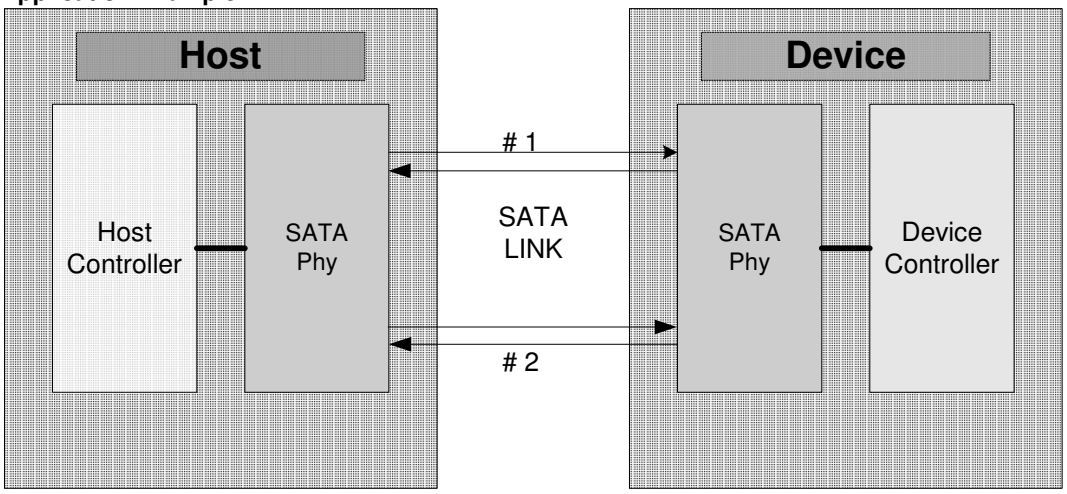
TRC6002CSA has a built-in Near and Far End Loopbacks. SLUMBER and PARTIAL Power Down feature minimize the power consumption of device.

TRC6002CSA is fabricated with TSMC's advanced 40 nm G CMOS logic process, and is portable to other processes.

Features

- Serial ATA fully compliant to Gen 1,Gen 2 and Gen3 SATA Phy Standards.
- Transmit and receive data at 1.5Gbps, 3.0 Gbps and 6.0 Gbps.
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution
- Jitter Tolerance is better than Specifications.
- 8bit/ or 10bit parallel interface logic.
- 8b/10b encoder and decoder
- High speed serial drivers
- High speed serial input stage with on-chip terminations
- Comma Detect for character alignment
- Far and Near End serial loopback test modes.
- Multi pattern generator and PRBS error checker to support BIST
- Three programmable levels of pre-emphasis and equalization.
- Standard OOB sequencing with optional bypassing OOB capability.
- 1.0V/1.8V ±5% Supply for logic core and control I/O.
- Low power, 120 mW max per channel.

Application Example:



Host: Storage System, Mother Board

Device: Disk Drive, Storage System

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Functional block diagram