Quad 3.125/6.25 Gbps Backplane SerDes IP Core

Description

TRC6204CBA is a Quad Serializer/Deserializer, which can operate as XAUI and double XAUI rate SerDes IP core. TRC6204CBA contains a low-jitter clock synthesizer, an 8/10-bit or 16/20 bit parallel to serial converter with built in 8b/10b encoder, and differential high speed Interface output ports. Its receive section contains an input limiting amplifier with on-chip terminations, a clock/data recovery PLL, a Comma detector, a serial to parallel converter with built-in 8b/10b decoder. Spread Spectrum Clocking (SSC) is used to minimize EMI and increase the quality of received signal. It has four levels of equalization at receiver, four level of pre-emphasis at transmitter, with built-in Near End and Far End retimed and local Loopbacks. Power management features are used to minimize the power consumption of device. Five different selectable patterns can be generated internally for testing. Extensive configuration and control features of TRC6204CBA make it very flexible for various applications and tests.

A built-in serial loopback mode, PRBS generator/checker and error detectors aid in support of testing.

The TRC6204CBA requires no external components for its clock synthesizers and clock recovery PLL's. Three external resistors are needed to set the proper bias currents for its on-chip terminations.

TRC6204CBA is fabricated with TSMC's 90 num advanced CMOS process and can be ported to other processes.

Features

- Quad SerDes optimized for Backplane applications
- Supports data rates 3.125 and 6.25 Gbps
- Comma Detect for character alignment
- Jitter Tolerance and Jitter Generation of device exceed specifications
- High-speed differential reference clock
- Low jitter clock synthesizers for clock distribution, ASIC clock for link layer, and SSC clock for reduced EMI
- 8b/10b encoder and decoder
- High speed serial CML output drivers with internal 50 Ω terminations
- High speed serial CML input stage with internal 50 Ω terminations
- Auto-calibration termination
- Supports up to four levels of pre-emphasis on the serial output drivers
- Supports up to four levels of equalization at the serial inputs
- Comma Detect for character alignment
- Near End and Far End retimed serial loopback Pseudo-Random (PRBS) pattern generator and error checker to support BIST
- Serial interface MDIO
- 1149.1 compatible JTAG port
- 1.0/1.8V ±5% supplies
- Power dissipation: 150 mW/Ch
- Power management modes
- TSMC advanced 90 nm CMOS process
- Portable to other processes

Figure 1. General Function Diagram

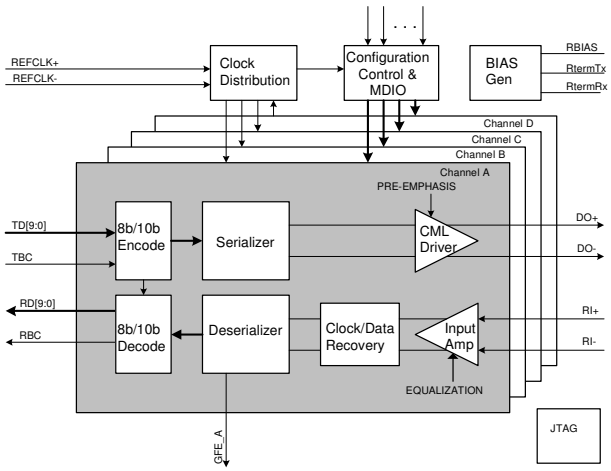

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Figure 2. Functional block diagram