## **TRC6254XRX IP Product Brief**

#### Description

TRC6254XRX is a 4 channel SERDES capable of providing XAUI (10G Attachment Unit Interface), RXAUI (10G Reduced Attachment Unit Interface) and SGMII interfaces. Fig. 1 shows the top-level block diagram of this module in the XAUI mode where these 4 channels can receive and transmit data synchronously at the rate of 3.125Gbps each. Fig. 2 shows the top-level block diagram of the module in RXAUI mode where 2 channels are disabled and the other 2 operate synchronously at the rate of 6.25Gbps each. The 4 channels can also operate as 4 independent channels.

Depending on the application, each transmitter can serialize 8, 10, 16 or 20 bit parallel data to a differential serial output and each receiver can de-serialize a differential serial input to 8, 10, 16 or 20 bit parallel output.

A common block including a TXPLL provides clocks to the serializers in all channels. To improve signal integrity the common block also includes a calibration circuit providing control signals to make the transmitter output resistance and the receiver input resistance within  $50\Omega \pm 10\%$ .

Fig 3. Shows the block diagram of each channel. At the RX side the serial input data goes through the input stage with linear equalization. The Clock and data recovery (CDR) circuit receives the data. It then extracts the clock, and provides the clock and the retimed data to the de-serializer. The de-serializer converts the serial data to 8, 10, 16 or 20bit parallel data with corresponding rx-clk.

There is an eye-monitor block to measure the height of the signal going to the CDR. When enabled, the information about the height of the signal will be sent out through 16 bit parallel data line.

A Loss Of Signal (LOS) detector also detects if there are valid data at the input.

For the boundary scan testing there is a AC JTAG block at the input providing data to the core in the test mode. At the TX side the serialized data goes through the output driver. To further improve the jitter performance there are programmable pre-emphasis capabilities at the transmitter output stage.

In addition near end and far end serial loopback are implemented to be able to test the channel.

### Features

- 4 channel SERDES capable of operating at 1.25, 2.5-3.125 and 5-6.25Gbps.
- Jitter generation and jitter tolerance meet SGMII, XAUI and RXAUI specifications.
- Serial output driver with calibrated on-chip termination resistor.
- Selectable pre-emphasis level of signal at the output driver.
- Serial input receiver with calibrated on-chip termination resistor.
- Fixed equalization capability at the receiver input.
- Near end and far end serial loopback.
- Loss of signal detector.
- Eye monitor
- AC JTAG
- Reference clock can be 25MHz or 156.25MHz.
- 2 power supplies of 0.9V and 1.2V.
- Only one external component is used (external resistor for termination resistor calibration).
- TSMC 40nm G process.









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Table 1 shows the speed of the clock and data at the parallel side for different applications based on 10 bit parallel data (and 20 bit for RXAUI mode).

### Table 1: Parallel interface speed

Mode	Serial Data rate	Parallel Data rate	Parallel Clock Frequency
RXAUI	6.25 Gbps	312.5Mbps	312.5 MHz
XAUI	3.125 Gbps	312.5Mbps	312.5 MHz
SGMII	1.25 Gbps	125Mbps	125 MHz



# Electrical Characteristics:

#	symbol	parameter	condition	Min	Тур	Max	Unit
1	TTD	Output Data Period		160		800	ps
2	VOD	Differential output swing	Minimum Maximum		800 1200		mV mV
3	PEM	Pre-emphasis ratio	Minimum Maximum		1 3		
4	RDO	Differential output resistance		90	100	110	Ohm

Table 2: TX output electrical characteristics:

## Table 3: TX Jitter generation

#	symbol	parameter	condition	Min	Тур	Max	Unit
1	RJ	Random jitter	RXAUI			8	mUI
		(ms)	XAUI			5	mUI
2	TJ	Total jitter	RXAUI			0.22	UI
		(PP)	XAUI			0.12	UI

Table 4: Electrical characteristics of the receiver input stage

#	symbol	parameter	condition	Min	Тур	Max	Unit
1	RTD	Input Data Period		160			ps
2	VID	Differential input swing		100		1500	mV
3	VCM	Input common mode	DC coupling		270		mV
4	RDI	Differential input resistance		90	100	110	Ohm

Table 5: RX Jitter tolerance for RXAUI

#	symbol	parameter	condition	Min	Тур	Max	Unit
1	RJ	Random jitter		0.2			UI
	+	+		+			
	DJ	Deterministic jitter +		0.37			UI
	+	Sinusoidal jitter for		+			
	SJ	f < 5MHz		0.1			UI

